IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): Dwyer et al.
Case: 6-14
Serial No.: 09/975,763
Filing Date: October 9, 2001
Group: 2188
Examiner: John A. Lane

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Signature: _____ Date: October 25, 2004

Title: Method and Apparatus for Cache Space Allocation

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith are the following documents relating to the above-identified patent application:

1. Appeal Brief (original and two copies); and
2. Copy of Notice of Appeal, filed on August 25, 2004, with copy of stamped return postcard indicating receipt of Notice by PTO on August 27, 2004.

There is an additional fee of $340 due in conjunction with this submission under 37 CFR §1.17(c). Please charge **Deposit Account No. 50-0762** the amount of $340, to cover this fee. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 50-0762** as required to correct the error. A duplicate copy of this letter and two copies of the Appeal Brief are enclosed.

Respectfully,

Date: October 25, 2004

Kevin M. Mason
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Signature: Gina Mauriz Date: October 25, 2004

Title: Method and Apparatus for Cache Space Allocation

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby appeal the final rejection dated May 6, 2004, of claims 1 through 30 of the above-identified patent application.

REAL PARTY IN INTEREST

The present application is assigned to Agere Systems Inc., as evidenced by an assignment recorded on October 9, 2001 in the United States Patent and Trademark Office at Reel 012262, Frame 0646. The assignee, Agere Systems Inc., is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1 through 30 are pending in the above-identified patent application. Claims 1, 10, 19, and 25 remain rejected under 35 U.S.C. §102(a and/or b) as being anticipated by the admitted prior art in co-pending related patent application

serial number 09/975,764 and claims 2-9, 11-18, 20-24, and 26-30 remain rejected under 35 U.S.C. §103(a) as being unpatentable over the admitted prior art in co-pending related patent application serial number 09/975,764.

STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the final rejection.

SUMMARY OF INVENTION

The present invention is directed to a method and apparatus for allocating a section of a cache memory to one or more tasks. A set index value that identifies a corresponding set in the cache memory is transformed to a mapped set index value that constrains a given task to the corresponding allocated section of the cache. The allocated cache section of the cache can be varied by selecting an appropriate map function. When the map function is embodied as a logical and function, for example, individual sets can be included in an allocated section, for example, by setting a corresponding bit value to binary value of one. A cache addressing scheme is also disclosed that permits a desired portion of a cache to be selectively allocated to one or more tasks. A desired location and size of the allocated section of sets of the cache memory may be specified.

ISSUES PRESENTED FOR REVIEW

i. Whether claims 1, 10, 19, and 25 are properly rejected under 35 U.S.C. §102(a and/or b) as being anticipated by the admitted prior art in co-pending related patent application serial number 09/975,764; and

ii. Whether claims 2-9, 11-18, 20-24, and 26-30 are properly rejected under 35 U.S.C. §103(a) as being unpatentable over the admitted prior art in co-pending related patent application serial number 09/975,764.

GROUPING OF CLAIMS

The rejected claims do not stand and fall together. More particularly, for the reasons given below, Applicants believe that each of the dependent claims

3/12/20/27, 4/13/21/28, 5/14/22, 8/17, and 9/18/24/30 provide independent bases for patentability apart from the rejected independent claims.

ARGUMENT

Independent claims 1, 10, 19, and 25 were rejected under 35 U.S.C. §102(a and/or b) as being anticipated by the admitted prior art in co-pending related patent application number 09/975,764. In particular, the Examiner asserts that the admitted prior art teaches "the frames/blocks in a set are allocated to a specific task while other frames/blocks in a different set are allocated to a different task." Furthermore, the Examiner asserts the admitted prior art's secondary tasks and primary task can only use allocated sets of the cache memory. In the Advisory Action dated August 4, 2004, the Examiner asserts that "all frames (locked or unlocked) within the cache are considered allocated."

The present invention is directed to allocating sets of cache memory to tasks. In particular, one or more secondary tasks may use only allocated sets of the cache memory. The allocation of such sets of cache memory restricts the access of the secondary tasks, such that the secondary tasks may use only the *allocated sets* of the cache memory; the secondary tasks may not use the unallocated sets (e.g., independent of whether the unallocated sets have been most recently used or not). The allocation may be performed before any cache accesses are performed, thereby preventing the access of unallocated sets by secondary tasks before any accesses to the cache occur.

The admitted prior art, alternatively, is directed to methods and apparatus for adaptively locking and unlocking *most recently used* frames in such cache memories. The admitted prior art does not allocate sets of a cache to control access of the cache by secondary tasks, but locks frames in response to a condition of being most recently used. The secondary tasks may utilize any frame that is not locked as a result of being most recently used. In fact, the admitted prior art teaches away from the present invention by teaching to allow secondary tasks to access any unlocked set of the cache. Independent claims 1, 10, 19, and 25, require wherein one or more secondary tasks may use *only* said *allocated sets* of said cache memory.

Thus, the admitted prior art does not disclose or suggest "wherein one or more secondary tasks may use only said allocated sets of said cache memory," as required by independent claims 1, 10, 19, and 25.

Conclusion

The rejections of the independent claims under section §102 in view of the admitted prior art are therefore believed to be improper and should be withdrawn.

Dependent Claims

Claims 3/12/20/27, 4/13/21/28, 5/14/22, 8/17, and 9/18/24/30 specify a number of limitations providing additional bases for patentability. Specifically, the Examiner rejected claims 3/12/20/27, 4/13/21/28, 5/14/22, 8/17, and 9/18/24/30 under 35 U.S.C. §103(a) as being unpatentable over the admitted prior art in co-pending related patent application serial number 09/975,764. Claims 3/12/20/27 require a mapper that transforms a set index, A, identifying a set in said cache memory to a mapped set index, a, identifying a set with said allocated portion of said cache memory. Claims 4/13/21/28 require wherein said allocated sets of said cache memory can be varied by selecting an appropriate map function. Claims 5/14/22 require wherein said map function is a logical and function and wherein a given set of said cache memory is allocated to a given task by assigning said set a predefined binary value. Claims 8/17 require wherein one of said allocated sections of sets of said cache memory may be specified using a section select value. Claims 9/18/24/30 require wherein a desired location and size of said allocated sections of sets of said cache memory may be specified.

Regarding the dependent claims, the Examiner asserts that the claim features, while part of the invention, appear to be well known and their relevance not essential to the main invention found in the independent claims. The Examiner further asserts that "it would have been obvious to one having ordinary skill in the art at the time of the invention to combine the admitted prior art with the officially taken prior art given the state of the art at the time the well known claim features were invented."

Applicants have reviewed the admitted prior art cited by the Examiner in the rejection of the dependent claims and could find no disclosure or suggestion of the limitations recited in the dependant claims.

Thus, the admitted prior art does not disclose or suggest a mapper that transforms a set index, A, identifying a set in said cache memory to a mapped set index, a, identifying a set with said allocated portion of said cache memory, as required by claims 3, 12, 20, and 27, does not disclose or suggest wherein said allocated sets of said cache memory can be varied by selecting an appropriate map function, as required by claims 4, 13, 21, and 28, does not disclose or suggest wherein said map function is a logical and function and wherein a given set of said cache memory is allocated to a given task by assigning said set a predefined binary value, as required by claims 5, 14, and 22, does not disclose or suggest wherein one of said allocated sections of sets of said cache memory may be specified using a section select value, as required by claims 8 and 17, and does not disclose or suggest wherein a desired location and size of said allocated sections of sets of said cache memory may be specified, as required by claims 9, 18, 24, and 30.

The remaining rejected dependent claims are believed allowable for at least the reasons identified above with respect to the independent claims.

The attention of the Examiner and the Appeal Board to this matter is appreciated.

Respectfully,

Date: October 25, 2004

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APPENDIX

1. A cache memory, comprising:

a plurality of sets of cache frames for storing information from main memory; and

a cache allocation system for allocating one or more sets of said cache memory to one or more tasks, wherein one or more secondary tasks may use only said allocated sets of said cache memory.

2. The cache memory of claim 1, wherein one or more primary tasks may use unallocated sets of said cache memory.

3. The cache memory of claim 1, further comprising a mapper that transforms a set index, A, identifying a set in said cache memory to a mapped set index, a, identifying a set with said allocated portion of said cache memory.

4. The cache memory of claim 1, wherein said allocated sets of said cache memory can be varied by selecting an appropriate map function.

5. The cache memory of claim 4, wherein said map function is a logical and function and wherein a given set of said cache memory is allocated to a given task by assigning said set a predefined binary value.

6. The cache memory of claim 1, further comprising a map register for identifying said one or more sets of said cache memory allocated to each task.

7. The cache memory of claim 1, wherein a size of said allocated one or more sets of said cache memory may be specified using a size select value.

8. The cache memory of claim 1, wherein one of said allocated sections of sets of said cache memory may be specified using a section select value.

9. The cache memory of claim 1, wherein a desired location and size of said allocated sections of sets of said cache memory may be specified.

10. A method for allocating space in a cache memory, said method comprising the steps of:

storing information from main memory in a plurality of sets of said cache memory; and

allocating one or more of said sets of said cache memory to one or more tasks, wherein one or more secondary tasks may use only said allocated sets of said cache memory.

11. The method of claim 10, wherein one or more primary tasks may use unallocated sets of said cache memory.

12. The method of claim 10, further comprising the step of transforming a set index, A, identifying a set in said cache memory to a mapped set index, a, identifying a set with said allocated portion of said cache memory.

13. The method of claim 10, further comprising the step of selecting an appropriate map function to vary said allocated sets of said cache memory.

14. The method of claim 13, wherein said map function is a logical and function and further comprising the step of allocating a given set of said cache memory to a given task by assigning said set a predefined binary value.

15. The method of claim 10, further comprising the step of identifying said one or more sets of said cache memory allocated to each task.

16. The method of claim 10, further comprising the step of specifying a size of said allocated one or more sets of said cache memory.

17. The method of claim 10, further comprising the step of specifying one of said allocated sections of sets of said cache memory.

18. The method of claim 10, further comprising the step of specifying a desired location and size of said allocated section of sets of said cache memory.

19. A cache memory, comprising:

means for storing information from main memory in a plurality of sets of said cache memory; and

means for allocating one or more of said sets of said cache memory to one or more tasks, wherein one or more secondary tasks may use only said allocated sets of said cache memory.

20. The cache memory of claim 19, further comprising means for transforming a set index, A, identifying a set in said cache memory to a mapped set index, a, identifying a set with said allocated portion of said cache memory.

21. The cache memory of claim 19, wherein said allocated sets of said cache memory can be varied by selecting an appropriate map function.

22. The cache memory of claim 21, wherein said map function is a logical and function and wherein a given set of said cache memory is allocated to a given task by assigning said set a predefined binary value.

23. The cache memory of claim 19, further comprising means for identifying said one or more sets of said cache memory allocated to each task.

24. The cache memory of claim 19, wherein a desired location and size of said allocated sections of sets of said cache memory may be specified.

25. An integrated circuit, comprising:

a cache memory having a plurality of sets of cache frames for storing information from main memory; and

a cache allocation system for allocating one or more sets of said cache memory to one or more tasks, wherein one or more secondary tasks may use only said allocated sets of said cache memory.

26. The integrated circuit of claim 25, wherein one or more primary tasks may use unallocated sets of said cache memory.

27. The integrated circuit of claim 25, further comprising a mapper that transforms a set index, A, identifying a set in said cache memory to a mapped set index, a, identifying a set with said allocated portion of said cache memory.

28. The integrated circuit of claim 25, wherein said allocated sets of said cache memory can be varied by selecting an appropriate map function.

29. The integrated circuit of claim 25, further comprising a map register for identifying said one or more sets of said cache memory allocated to each task.

30. The integrated circuit of claim 25, wherein a desired location and size of said allocated sections of sets of said cache memory may be specified.

COPY

Ryan, Mason & Lewis, LLP
ATTORNEYS AT LAW
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FAIRFIELD, CT 06824

Receipt in the USPTO is hereby acknowledged of:

Transmittal Letter – (Original & 1 copy)
Notice of Appeal - (Original & 1 copy)
Petition for Extension of Time (Original & 1 copy)

Case Name: Dwyer 6-14
Serial No.: 09/975,763

1150-1031

August 25, 2004 KMM

PTO/SB/31 (02-01)
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NOTICE OF APPEAL FROM THE EXAMINER TO THE BOARD OF PATENT APPEALS AND INTERFERENCES	Docket Number (Optional) Dwyer 6-14

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Signature: Tina Maurice

Typed or printed name: Tina Maurice

In re Application of	
Dwyer et al.	
Application Number	**Filed**
09/975,763	October 9, 2001
For Method and Apparatus for Cache Space Allocation	
Group Art Unit	**Examiner**
2188	John A. Lane

Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the examiner.

The fee for this Notice of Appeal is (37 CFR 1.17(b)) $330.00.

- ☐ Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee shown above is reduced by half, and the resulting fee is: $_____.
- ☐ A check in the amount of the fee is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Commissioner has already been authorized to charge fees in this application to a Deposit Account. I have enclosed a duplicate copy of this sheet.
- ☑ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 50-0762. I have enclosed a duplicate copy of this sheet.
- ☑ A petition for an extension of time under 37 CFR 1.136(a) (PTO/SB/22) is enclosed.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☑ attorney or agent of record.
- ☐ attorney or agent acting under 37 CFR 1.34(a). Registration number if acting under 37 CFR 1.34(a)._____.

Kevin M. Mason
Signature

Kevin M. Mason
Typed or printed name

August 25, 2004
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.